LISTING OF THE CLAIMS

The listing of claims will replace all prior versions and listings of claims in the application:

1. **(Previously Presented)** In a system that includes a master component that is configured to communicate with one or more slave components over a clock wire and a data wire, a method for the master component communicating over the data wire while enabling recovery of synchronization between the master component and the one or more slave components, the method comprising the following:

determining that an operation is to be performed on a slave component of the one or more slave components;

monitoring the data wire of the two-wire interface upon determining that the operation is to be performed on the slave component;

detecting at least a predetermined number of consecutive bits of the same binary polarity have occurred on the data wire while monitoring the data wire; and

asserting a frame of the two-wire interface on the data wire in response to detecting that the predetermined number of consecutive bits of the same polarity have occurred on the data wire.

2. **(Original)** A method in accordance with Claim 1, wherein the two-wire interface is a guaranteed header two-wire interface.

3. **(Original)** A method in accordance with Claim 1, wherein the two-wire interface is not a guaranteed header two-wire interface.

4. **(Previously Presented)** A method in accordance with Claim 1, wherein detecting at least the predetermined number of consecutive bits comprises the following:

detecting at least the predetermined number of consecutive bits of a logical one.

5. **(Original)** A method in accordance with Claim 4, wherein the data wire is pulled high when no components are asserting binary values on the data wire.

6. **(Previously Presented)** A method in accordance with Claim 1, wherein detecting at least the predetermined number of consecutive bits comprises the following:

detecting at least the predetermined number of consecutive bits of a logical zero.

7. **(Original)** A method in accordance with Claim 6, wherein the data wire is pulled low when no components are asserting binary values on the data wire.

8. **(Previously Presented)** A method in accordance with Claim 1, further comprising the following:

asserting, at the master component, a clock signal on the clock wire during at least some of the act of monitoring the data wire.

9. **(Previously Presented)** A method in accordance with Claim 1, further comprising the following:

asserting, at the master component, a voltage level on the data wire during only a portion of the act of monitoring the data wire.

10. **(Original)** A method in accordance with Claim 9, wherein the data wire is pulled high when no components are asserting binary values on the data wire.

11. **(Original)** A method in accordance with Claim 9, wherein the data wire is pulled low when no components are asserting binary values on the data wire.

12. **(Previously Presented)** A method in accordance with Claim 1, further comprising the following:

refraining from asserting, at the master component, a voltage level on the data wire while monitoring the data wire.

13. **(Original)** A method in accordance with Claim 12, wherein the data wire is pulled high when no components are asserting binary values on the data wire.

14. **(Original)** A method in accordance with Claim 12, wherein the data wire is pulled low when no components are asserting binary values on the data wire.

15. **(Previously Presented)** A method in accordance with Claim 1, wherein determining that an operation is to be performed on a slave component of the one or more slave components comprises the following:

determining that a read operation is to be performed with an extended address as compared to other frames communicated over the data wire.

16. **(Previously Presented)** A method in accordance with Claim 1, wherein determining that an operation is to be performed on a slave component of the one or more slave components comprises the following:

determining that a write operation is to be performed with an extended address as compared to other frames communicated over the data wire.

17. **(Previously Presented)** A method in accordance with Claim 1, wherein determining that an operation is to be performed on a slave component of the one or more slave components comprises the following:

determining that a read operation is to be performed with a shorter address as compared to other frames communicated over the data wire.

18. **(Previously Presented)** A method in accordance with Claim 1, wherein determining that an operation is to be performed on a slave component of the one or more slave components comprises the following:

determining that a write operation is to be performed with a shorter address as compared to other frames communicated over the data wire.

19. **(Previously Presented)** A method in accordance with Claim 1, wherein determining that an operation is to be performed on a slave component of the one or more slave components comprises the following:

determining that a read operation is to be performed with cyclic redundancy checking over the data wire.

20. **(Previously Presented)** A method in accordance with Claim 1, wherein determining that an operation is to be performed on a slave component of the one or more slave components comprises the following:

determining that a write operation is to be performed with cyclic redundancy checking over the data wire.

21. **(Previously Presented)** A method in accordance with Claim 1, wherein determining that an operation is to be performed on a slave component of the one or more slave components comprises the following:

determining that a read operation is to be performed with acknowledgements over the data wire.

22. **(Previously Presented)** A method in accordance with Claim 1, wherein determining that an operation is to be performed on a slave component of the one or more slave components comprises the following:

determining that a write operation is to be performed with acknowledgements over the data wire.

23. **(Previously Presented)** A system comprising the following:

a master component;

a slave component;

a clock wire interconnected between the master component and the slave component;

a data wire interconnected between the master component and the slave component,

wherein the master component is configured to perform the following:

determining that an operation is to be performed on the slave component;

monitoring the data wire of the two-wire interface upon determining that the operation is to be performed on the slave component;

detecting at least a predetermined number of consecutive bits of the same binary polarity have occurred on the data wire while monitoring the data wire; and

asserting a frame of the two-wire interface on the data wire in response to detecting that the predetermined number of consecutive bits of the same polarity have occurred on the data wire.

24. **(Original)** A system in accordance with Claim 23, wherein the two-wire interface is a guaranteed header two-wire interface.

25. **(Original)** A system in accordance with Claim 23, wherein the two-wire interface is not a guaranteed header two-wire interface.

26. **(Original)** A system in accordance with Claim 23, wherein the data wire is pulled high when no components are asserting binary values on the data wire.

27. **(Original)** A system in accordance with Claim 23, wherein the data wire is pulled low when no components are asserting binary values on the data wire.

28. **(Previously Presented)** A master component that is configured to do the following when coupled to a slave component via a clock wire and a data wire:

determining that an operation is to be performed on the slave component;

monitoring the data wire of the two-wire interface upon determining that the operation is to be performed on the slave component;

detecting at least a predetermined number of consecutive bits of the same binary polarity have occurred on the data wire while monitoring the data wire; and

asserting a frame of the two-wire interface on the data wire in response to detecting that the predetermined number of consecutive bits of the same polarity have occurred on the data wire.

29. **(Original)** A master component in accordance with Claim 28, wherein the two-wire interface is a guaranteed header two-wire interface.

30. **(Original)** A master component in accordance with Claim 28, wherein the two-wire interface is not a guaranteed header two-wire interface.

31. **(Original)** A master component in accordance with Claim 28, wherein the master component is implemented in a laser transmitter/receiver.

32. **(Original)** A master component in accordance with Claim 31, wherein the laser transmitter/receiver is a 1G laser transceiver.

33. **(Original)** A master component in accordance with Claim 31, wherein the laser transmitter/receiver is a 2G laser transceiver.

34. **(Original)** A master component in accordance with Claim 31, wherein the laser transmitter/receiver is a 4G laser transceiver.

35. **(Original)** A master component in accordance with Claim 31, wherein the laser transmitter/receiver is a 10G laser transceiver.

36. **(Original)** A master component in accordance with Claim 31, wherein the laser transmitter/receiver is a laser transceiver suitable for fiber channels greater than 10G.

37. **(Original)** A master component in accordance with Claim 31, wherein the laser transmitter/receiver is an XFP laser transceiver.

38. **(Original)** A master component in accordance with Claim 31, wherein the laser transmitter/receiver is an SFP laser transceiver.

39. **(Original)** A master component in accordance with Claim 31, wherein the laser transmitter/receiver is a SFF laser transceiver.

40. **(Previously Presented)** A master component in accordance with Claim 1, further comprising the following:

interspersing a bit at a guaranteed minimum frequency among data transmitted on the data wire,

wherein the interspersed bit is of a polarity opposite that of the detected predetermined number of consecutive bits.